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Chapter 1 : List of series integrated circuits - Wikipedia

Davidson Every shop needs a well regulated variable voltage power supply for bench top work. Some use a door laid flat across some saw horses as a start. Building a real sturdy workbench out of two by four lumber is better. A nice long electrical outlet strip is also most a must. You can see what I mean in the picture at the left. The outlet strip is just below the row of colored plastic bins. A shelf on your workbench to hold your test equipment is also nice. Also, notice the light above the workbench - also a must. You can also add swinging lamps as well. If you can afford it you can purchase a nice workbench like in the picture already built. A good sturdy stool or chair is a must as well. Lots of additional shelving and storage boxes will help you sort out parts you may have and keep the labeled for easy location when you need them. Try to keep your workbench free after you complete a job or project. Otherwise you will end up with no bench top space left to start new projects. That is why additional shelf and storage is a must. If you follow these rules you will have a nice looking as well as an efficient place to work. Carpet on the floor is a no-no because of static electricity it can generate. Also add a waste basket and a metal storage bin or cabinet of some sort to store chemicals. You will collect control cleaner, glues and various other chemicals that need proper and safe storage A separate workbench could be added for drilling and other metal working. A nice vise, grinding wheels, and drill press are necessary at times for building metal enclosure boxes. Enjoy your new workbench and work space!

Chapter 2 : ELECTRONICS PAGE 2 - blog.quintoapp.com

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Combinational synthesis This section lists combinational synthesis commands implemented in the current release. Rewriting is performed using a library of pre-computed four-input AIGs command rewrite; standard alias rw , or collapsing and refactoring of logic cones with inputs command refactor; standard alias rf. It can be experimentally shown that iterating these two transformations and interleaving them with AIG balancing command balance; standard alias b substantially reduces the AIG size and tends to reduce the number of AIG levels. The logic synthesis scripts currently offered are resyn, resyn2, and resyn2rs. They are defined as aliases in the resource file abc. Although these scripts do not include a dedicated command to extract common logic, the logic is being shared due to the DAG-aware nature of rewriting. It accepts changes only if the number of the AIG nodes is reduced, which is achieved by restructuring the current AIG and maximally sharing the other nodes available in the current network. This is especially true if rewrite and refactor are used with a switch enabling zero-cost replacements, as in the above scripts commands rewrite â€”z and refactor â€”z; standard aliases rwz and rfz, respectively. In this case, even if rewriting does not immediately reduce the AIG size, the structure is reshaped and new opportunities for logic sharing are created for the future rewriting iterations. Other synthesis commands can be used to convert initial SOP logic network into an AIG using structural hashing command strash; standard alias st and recreating SOP logic network from the AIG command renode; standard alias ren. The traditional fast extract command fx can be applied to the SOP logic network, as well as DSD-based sharing extraction scripts share and sharedsd, respectively. In our experience, these commands do not perform as well as AIG rewriting when it comes to reducing both the number of nodes area and the number of logic levels delay. Combinational logic synthesis in ABC using resyn and resyn2 is typically x faster compared to script. In ABC, the node boundaries are initially destroyed by structural hashing command strash , which transforms a logic network into an AIG. The boundries can be recreated on demand using command renode, which can be seen as a reverse of the SIS command eliminate. In the synthesis flow presented above scripts resyn and resyn2 logic is transformed on the AIG level without creating nodes. In a sense, ABC works on a completely eliminated network, in which node boundaries do not exist whereas other tools preserve the node boundaries. The inverters do not count towards the number of logic levels. The balancing is applied in the topological order and selects the minimum delay tree-decomposition of each multi-input AND-gate. Balancing takes into account the arrival times of primary inputs, which can be represented in BLIF. Collapsing is performed by building global functions using BDDs and is, therefore, limited to relatively small circuits. After collapsing, the node functions are represented using BDDs. Creates node boundaries in this AIG and collapses the intermediate logic to form larger nodes. The resulting AIG is a logic network composed of two-input AND gates and inverters represented as complemented attributes on the edges. Structural hashing is a purely combinational transformation, which does not modify the number and positions of latches. Sweep performs the following tasks: Sweep cannot be applied to an AIG because an AIG is structurally hashed and therefore does not have buffers, inverters, and unpropagated constant nodes. To remove dandling nodes in the logic network, use cleanup. Sequential synthesis Sequential synthesis transforms the current network by modifying its logic together with the memory elements latches or flip-flops if they are present. The resulting network may have a different state encoding and reachable state space, compared to the original network, but the two networks are sequentially equivalent that is, starting from the initial states, for the same sequences of input vectors, they produce identical sequences of the output vectors. The simplest sequential transformation is retiming. More complex sequential transformations modify both the logic structure and the positions of the latches. A special place among sequential transformations is given to integrated sequential optimization , which can achieve the globally optimal delay of the circuit by performing a sequence of simple local transformations, such as local restructuring and retiming individual nodes. In ABC

integrated sequential optimization is current performed by command if -s. This command finds the minimum delay for the circuit, by exploring the combined space of all logic structures seen during logic synthesis, all possible technology mappings, and all possible retimings. Currently, only a simple delay-optimal version of sequential integration is implemented in the commands if -s, without much effort to minimize the number of registers and the area of the resulting mapping. However, the resulting area is often larger. This is a known limitation of the current implementation. It will be addressed in the future work by developing efficient latch-minimization and area-recovery techniques based on the notion of sequential slack. Detects and merges sequentially equivalent registers. The latches are optimally shared across the fanout stems when the circuit is transformed from the sequential AIG into a logic network. The computation of initial states after retiming is reduced to a SAT problem, which is solved using MiniSat. When used with switch â€”l e. Detects and merges sequentially equivalent nodes. The registers are transformed by adding a pair of inverters at the output of the register and retiming the register forward over the first inverter. Note that some of these commands are applicable to AIGs and some are applicable to logic networks. To convert between the two, use strash and logic.

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Overview[edit] Some TTL logic parts were made with an extended military-specification temperature range. These parts are prefixed with 54 instead of 74 in the part number. A short-lived 64 prefix on Texas Instruments parts indicated an industrial temperature range; this prefix had been dropped from the TI literature by Surface mount parts with a single gate often in a 5-pin or 6-pin package are prefixed with G instead of Some manufacturers released some series equivalent CMOS circuits with a 74 prefix, for example the 74HC was a replacement for the with slightly different electrical characteristics different power supply voltage ratings, higher frequency capabilities, lower "on" resistances in analog switches, etc. See List of series integrated circuits. Conversely, the series has "borrowed" from the series - such as the CD and CD being pin-for-pin functional replacements for 74C and 74C A few alphabetic characters to designate a specific logic subfamily may immediately follow the 74 or 54 in the part number, e. Not all functions are available in all families. In a few instances, such as the and , the same suffix in different families do not have completely equivalent logic functions. Another extension to the series is the xxx variant, representing mostly the bit wide counterpart of otherwise 8-bit-wide "base" chips with the same three ending digits. For more details, refer primarily to the Texas Instruments documentation mentioned in the References section. There are a few numeric suffixes that have multiple conflicting assignments, such as the Larger footprints[edit] Parts in this section have a pin count of 14 pins or more. The lower part numbers were established in the s and s, then higher part numbers were added incrementally over decades. IC manufacturers continue to make a core subset of this group, but many of these part numbers are considered obsolete and no longer manufactured. Older discontinued parts may be available from a limited number of sellers as new old stock NOS , though some are much harder to find. For the following table: Part number column - the "x" is a place holder for the logic subfamily name. For example, 74x00 in "LS" logic family would be "74LS00". Input column - a blank cell means a normal input for the logic family type. Outputs with higher output currents are often called drivers or buffers. Pins column - number of pins for the dual in-line package version; a number in brackets indicates that there is no known dual in-line package version of this IC 74x00 â€” 74x

Chapter 4 : List of integrated circuit packaging types - Wikipedia

Advances in integrated-circuit technology are making practical new orders of magnitude in electronic equipment complexity, performance, and reliability. This paper describes design principles, fabrication techniques, and application considerations for monolithic integrated circuits, in which both.

Chapter 5 : - Abc's of integrated circuits, by Rufus P Turner

A fine book for a collector/student/scientist of the earlier days of integrated circuit development. Fantastic, easily readable introduction to integrated circuits. Even though this classic text is from the earlier days of the IC, it is ideal for the student just learning about the basics.

Chapter 6 : ABC: A Simple System for Sequential Synthesis and Verification

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